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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/632,713	08/01/2003	Hiroshi Takeda	NEC 03FN020	2805

27667 7590 12/13/2005

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EXAMINER	
LIANG, REGINA	
ART UNIT	**PAPER NUMBER**
2674	

DATE MAILED: 12/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/632,713	TAKEDA ET AL.	
	Examiner	Art Unit	
	Regina Liang	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *2,4,6 and 8* is/are allowed.

6)☒ Claim(s) *1,3,5 and 7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 11/2/05, 8-1-03
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Hirai et al (JP 10-293559 hereinafter Hirai).

Fig. 1 of Hirai discloses an active matrix LCD configured to invert a polarity of a voltage on a common electrode (17) by row or by frame, comprising a common voltage supply circuit (common electrode drive circuit 28 as shown in Figs. 2 and 3) provided to supply a common voltage Vcom to the common electrode (17, section [0022] of the English translation), a charge collection and resupply circuit (charge reuse circuits 31, 32) connected between the common electrode and the common voltage supply circuit. Fig. 2 of Hirai teaches the charge collection and resupply circuit (charge reuse circuits 31, 32) including: a first switch (sw111) connected between the common electrode (17) and the common voltage supply circuit; a charge collection capacitor (c11); a second switch (sw122) connected between a connection point (point at 29) of the common electrode and the first switch and the charge collection capacitor; a switch control unit (Fig. 4) provided to control turning on and off of the first and second switches, the switch control unit being configured to operate such that immediately before a polarity of common voltage Vcom is inverted, the first switch (sw111) is turned off and then the second switch (sw122) is turned on (at time period t11), the further, after inversion of the polarity of the

common voltage Vcom, the second switch is turned off and then the first switch is turned on (at time period t12, see sections [0034]-[0038] of the English translation).

Claim Rejections - 35 USC § 103

3. Claim 3, 5, 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirai in view of Harada (JP 02002041003).

As to claims 3, 5, Hirai does not disclose the device comprising a DC level shift circuit for inverting a polarity of a common voltage. However, Harada teaches a LCD device having a common signal generating circuit (16) which including a DC level shift circuit (see Fig. 2) for inverting a polarity of a common voltage (Vcom). Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Hirai to have a DC level shift circuit for inverting a polarity of a common voltage as taught by Harada since the amplitude of the common signal Vcom is suppressed to about a power source voltage for driving a logic circuit so as to reduce power consumption.

Hirai as modified by Harada does not explicitly disclose the DC level shift circuit disposed in a stage prior to the charge collection and resupply circuit or in a stage subsequent to the charge collection and resupply circuit. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the DC level shift circuit of Hirai as modified by Harada to be disposed in a stage prior to the charge collection and resupply circuit or in a stage subsequent to the charge collection and resupply circuit, since it has been held that rearranging parts of an invention involves only routine skill in the art. *In re Japikse*, 86 USPQ 70.

As to claim 7, Fig. 2 of Harada shows the DC level shift circuit includes a capacitor, a firs bias voltage generation resistor, and a second bias voltage generation resistor as claimed.

Allowable Subject Matter

4. Claims 2, 4, 6 and 8 are allowed.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Makishima et al (US. PAT. NO. 6,812,911) teaches a LCD device.

Yasui et al (US. PAT. NO. 5,831,605) teaches LCD device with stabilized common potential.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Regina Liang whose telephone number is (571) 272-7693. The examiner can normally be reached on Monday-Friday from 8AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick Edouard, can be reached on (571) 272-7603. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Regina Liang
Primary Examiner
Art Unit 2674

12/9/05